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EXAMINER

LIN, KENNY S

ART UNIT	PAPER NUMBER
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2154

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/606,899

Applicant(s)

BENAYOUN ET AL.

Examiner

Kenny Lin

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 June 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6 is/are allowed.
- 6) ☒ Claim(s) 1-5 and 7-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-15 are presented for examination.

Allowable Subject Matter

2. Claim 6 is allowable.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blelloch, US 6,434,590, in view of Chen et al (hereinafter Chen), US 5,440,740.

5. Blelloch and Chen were cited in the previous office action.

6. As per claim 1, Blelloch taught the invention substantially as claimed including a hardware device for concurrently processing a plurality of tasks associated with an algorithm which includes a number of processes some of which are dependant on binary decisions (col.2, lines 29-60) said device comprising:

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- a. A plurality of task units for processing data, making decisions and/or processing data and making decisions (col.2, lines 45-46);
- b. A task interconnection logic means interconnecting the task units for communicating actions from a source task unit to a destination task unit (col.2, lines 46-55, 61-67, col.3, lines 1-8, 10-15, an interconnection logic means is inherently needed in communicating between source task unit and destination task units).
- c. Each of said task units including a processor for executing the steps of the associated task in response to a received request action (col.2, lines 46-55); and
- d. one status manger for handling actions from source task units and building actions to be sent to destination task units (col.2, lines 43-48).

7. Blleloch did not specifically teach each task units to include a status manager. However, Blleloch taught that the processing elements execute the instructions of the tasks from the assignment manager and inform the assignment manager when the tasks are completed (col.2, lines 52-55). Chen taught to include status managers in each task unit for handling actions from source task units and building actions to be sent to destination task units (col.11, lines 61-68, col.12, lines 1-28; intertask control blocks). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blleloch and Chen because Chen's teaching of using status managers in teach task units enables Blleloch's device to pass status and control information between tasks (see Chen, col.11, lines 61-68, col.12, lines 1-28).

8. As per claim 11, Blleloch and Chen taught the invention substantially as claimed in claim

1. Blleloch further taught wherein each task unit of the plurality of task units is configured to perform only one task of the plurality of tasks associated with the algorithm.

9. As per claim 12, Blleloch taught the invention substantially as claimed including a hardware device for concurrently processing a plurality of tasks associated with an algorithm (col.2, lines 29-60), comprising:

- a. At least two task units each configured to process the steps of a respective single task of a multiple task algorithm (col.2, lines 45-46);
- b. At least two processors configured to execute the respective single task in each of the respective at least two task units (col.2, lines 45-46);
- c. An interconnection logic means for routing actions from a source task unit to a destination task unit of the at least two task units, respectively (col.2, lines 30-32, fig.1); and
- d. A status managers being associated with each of the at least two task units (col.2, lines 43-57, 61-67, col.3, lines 1-8).

10. Blleloch taught to use one status manager in associating with the task units in the processing system (col.2, lines 43-60) where the status manager receive actions from the interconnection logic means and directing execution of the single task (col.2, lines 52-55).

Blleloch did not specifically teach at least two status managers each being associated with each

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of the at least two task units, respectively. Chen taught to include status managers in each task unit for handling actions from source task units and building actions to be sent to destination task units (col.11, lines 61-68, col.12, lines 1-28; intertask control blocks). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blleloch and Chen because Chen's teaching of using status managers in teach task units enables Blleloch's device to pass status and control information between tasks (see Chen, col.11, lines 61-68, col.12, lines 1-28).

11. As per claim 13, Blleloch and Chen taught the invention substantially as claimed in claim

12. Blleloch further taught wherein each of the task units repetitively perform only its respective single task (col.2, lines 55-57).

12. As per claim 14, Blleloch and Chen taught the invention substantially as claimed in claim

13. Blleloch further taught that wherein the status manager handles incoming commands for other task units of the at least two task units and builds commands to be sent to one of the other task units (col.2, lines 43-48).

13. As per claim 15, Blleloch and Chen taught the invention substantially as claimed in claim

14. Blleloch further taught wherein the source task unit is configured to activate the destination task unit (col.2, lines 30-32, 38-48).

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14. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blelloch and Chen as applied to claim 1 above, and further in view of "Official Notice".

15. As per claim 2, Blelloch and Chen taught the invention substantially as claimed in claim

1. Blelloch further taught that wherein said actions communicated from a source task unit to a destination task unit are START used to activate the processor of said destination task unit (col.2, lines 52-55) and VALID used to confirm that task associated with said destination task unit corresponds to a decision included in said task (col.3, lines 26-27). Blelloch and Chen did not specifically teach the actions to include KILL used to cancel the task associated with said destination task unit. However, "Official Notice" is taken that it would have been obvious to add different actions to perform desired actions according to administrating needs. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement Blelloch and Chen's system with actions such as KILL and PAUSE to perform administrative actions.

16. As per claim 3, Blelloch and Chen taught the invention substantially as claimed in claim

2. Blelloch further taught that wherein said status manager activates said processor for processing the steps of the task associated with said destination task unit when the action received from a source task unit is START (col.2, lines 61-67, col.3, line 1).

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17. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blelloch and Chen as applied to claim 3 above, and further in view of Papadopoulos et al (hereinafter Papadopoulos), US 5,430,850.

18. Papadopoulos was cited in the previous office action.

19. As per claim 4, Blelloch and Chen taught the invention substantially as claimed in claim 3. Blelloch and Chen did not specifically teach that the wherein said status manager is a state machine. Papadopoulos taught that the status manager is a state machine (col.26, lines 54-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blelloch and Papadopoulos because Papadopoulos' teaching of using a state machine as the status manager enables the status manager in Blelloch's device to consume messaging abilities.

20. Claims 5, 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blelloch and Chen as applied to claim 3 above, and further in view of Papadopoulos et al (hereinafter Papadopoulos), US 5,430,850 and "Official Notice".

21. As per claim 5, Blelloch and Chen taught the invention substantially as claimed in claim 3. Blelloch and Chen did not specifically teach that wherein each of said task units further comprises a plurality of control/data registers each corresponding, for the task associated with said task unit, to an instance of the algorithm flow (col.5, lines 24-39). Papadopoulos taught

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that wherein each of said task units further comprises a plurality of control/data registers each corresponding, for the task associated with said task unit, to an instance of the algorithm flow (col.5, lines 24-39). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blleloch, Chen and Papadopoulos because Papadopoulos' teaching of having a plurality of control/data register in the task units provides Blleloch's device address registration abilities. Blleloch, Chen and Papadopoulos did not specifically teach that each one of said control/data registers comprising a control field composed of a completion bit set to 1 when the associated task is completed, a validation bit set to 1 when the associated task is validated and a L/R bit indicating that the output in the algorithm flow is left or right when said task includes a decision. However, Official Notice is taken that both the concept and advantage of using bits in data register is well known and expected in the art. It would have been obvious to use bits in data register to indicate the condition of the associated task. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use specific bit(s) to indicate the status of the task in Blleloch, Chen and Papadopoulos' system according to design choice.

22. As per claim 7, Blleloch, Chen and Papadopoulos taught the invention substantially as claimed in claim 5. Blleloch, Chen and Papadopoulos did not specifically teach that wherein said completion bit is sent by said processor to said status manager after completion of the task execution. However, Official Notice is taken that both the concept and advantage of using notification is well known and expected in the art. Blleloch taught to send acknowledgement to the status manager to inform task completion (col.3, lines 26-37). It is obvious to send

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notifications to notify the status manager of the current status. It would have been obvious to one of ordinary skill in the art at the time the invention was made to send a completion bit to the status manager in Blelloch, Chen and Papadopoulos' system to notify the completion of task execution in the system.

23. As per claim 8, Blelloch, Chen and Papadopoulos taught the invention substantially as claimed in claim 5. Blelloch, Chen and Papadopoulos did not specifically teach that wherein said control/data register corresponding to a specific instance is cleared by said status manager when this one receives an action KILL for the task associated with said task unit and for said specific instance. However, Official Notice is taken that both the concept and advantage of using a KILL/Delete action is well known and expected in the art. It would have been obvious that the objective of a KILL/Delete action is to remove a specific instance. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a KILL action in Blelloch, Chen and Papadopoulos's system to clear a specific instance.

24. In response to applicant's challenge, Van Dyke et al, US 6,412,070, filed September 21, 1998 disclose the use of KILL command (col.5, lines 25-35). This evidence proves that the Official Notice was properly taken and it would be obvious to provide KILL/Delete command in the system. It would have been obvious that the objective of a KILL/Delete action is to remove a specific instance. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a KILL action in Blelloch, Chen and Papadopoulos's system to clear a specific instance (see Final Office action dated on 10/15/04, response to argument point 4).

25. As per claim 9, Blelloch, Chen and Papadopoulos taught the invention substantially as claimed in claim 5. Blelloch, Chen and Papadopoulos did not specifically teach that wherein each of said task units further comprises two configuration registers CONFIG.L and CONFIG.R which are respectively selected by the binary value of said bit L/R of the control/data register of the instance being considered, the contents of said configuration registers being loaded at the beginning of the algorithm processing for defining the task to be activated, the action to be performed and the instance to be considered. However, Official Notice is taken that both the concept and advantage of using of CONFIG.L and CONFIG.R registers is well known and expected in the art. It would have been obvious to use them to define the tasks that need to be activated. It would have been obvious to use CONFIG.L and CONFIG.R in Blelloch, Chen and Papadopoulos' system as the configuration registers to define the tasks, actions and instances.

26. In response to applicant's challenge, Brown, US 3,914,744, filed January 2, 1973 disclosed a control register using L/R bit to direct the direction (col.3, lines 42-47). It would have been obvious to use CONFIG.L and CONFIG.R in Blelloch, Chen and Papadopoulos' system as the configuration registers to define the tasks, actions and instances (see Final Office action dated on 10/15/04, response to argument point 4).

27. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blelloch, Chen and Papadopoulos as applied to claims 1-9 above, and further in view of Fairfield et al (hereinafter Fairfield), US 5,321,842.

28. Fairfield was cited in the previous office action.

29. As per claim 10, Blelloch, Chen and Papadopoulos taught the invention substantially as claimed in claim 5. Blelloch, Chen and Papadopoulos did not specifically teach that wherein said task interconnection logic means is composed of three-state drivers each one of said drivers being associated with one of said tasks as input task and a number of buses equal to the number of said tasks as output tasks, one of said buses being selected by the driver corresponding to an input task after decoding an action word by said driver. However, the use of three-state driver is well known in the art and would have been obvious to implement the task interconnection logic means with three-state drivers. Fairfield taught a processor using three-state drivers (col.2, lines 4-16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blelloch, Chen and Papadopoulos and Fairfield because Fairfield's teaching of using three-state drivers help to employ feedback to the processor in Blelloch, Chen and Papadopoulos' system.

Response to Arguments

30. Applicant's arguments filed 6/17/2005 have been fully considered but they are not persuasive.

31. In the remark, applicant argued (1) Blelloch does not teach or suggest that each task unit includes a processor. (2) Blelloch does not teach or suggest a task interconnection logic means

interconnecting the task units ... each of said task units including a processor ... a status manager for handling actions from source task units and building actions to be sent to destination task units. (3) Chen, Papadopoulos and Fairfield fails to teach or suggest a plurality of task units, in which each task unit includes a processor. (4) There is no motivation or suggestion in combining the references. (5) Applicant challenge examiner's Official Notice to provide factual basis to claims 2-3, 5 and 7-9.

32. As to point (1), Blleloch taught to include a plurality of processing elements for processing tasks (task units). It is inherently known that processing elements are use for processing. Therefore, be definition, processing elements are processors.

33. As to point (2), Blleloch taught the invention substantially as claimed including a hardware device for concurrently processing a plurality of tasks associated with an algorithm which includes a number of processes some of which are dependant on binary decisions (col.2, lines 29-60) said device comprising: a plurality of task units for processing data, making decisions and/or processing data and making decisions (col.2, lines 45-46); a task interconnection logic means interconnecting the task units for communicating actions from a source task unit to a destination task unit (col.2, lines 46-55, 61-67, col.3, lines 1-8, 10-15, an interconnection logic means is inherently needed in communicating between source task unit and destination task units). Each of said task units including a processor for executing the steps of the associated task in response to a received request action (col.2, lines 46-55) and one status manger for handling actions from source task units and building actions to be sent to destination task units (col.2, lines 43-48). Blleloch did not specifically teach each task units to include a

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status manager. However, Blelloch taught that the processing elements execute the instructions of the tasks from the assignment manager and inform the assignment manager when the tasks are completed (col.2, lines 52-55). Chen taught to include status managers in each task unit for handling actions from source task units and building actions to be sent to destination task units (col.11, lines 61-68, col.12, lines 1-28; intertask control blocks). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blelloch and Chen because Chen's teaching of using status managers in each task unit enables Blelloch's device to pass status and control information between tasks (see Chen, col.11, lines 61-68, col.12, lines 1-28).

As to point (3), in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Blelloch taught to include a plurality of task units each having processor.

As to point (4), Chen specifically point out the advantage and motivation in combining with Blelloch (see Chen, col.11, lines 61-68, col.12, lines 1-28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blelloch and Chen because Chen's teaching of using status managers in each task unit enables Blelloch's device to pass status and control information between tasks (see Chen, col.11, lines 61-68, col.12, lines 1-28). In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where

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there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, motivation can be found in the knowledge generally available to one of ordinary skill in the art. One of ordinary skill in the art would have been motivated to use multi-functional machine or devices to further benefit the system. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blelloch and Papadopoulos because Papadopoulos' teaching of using a state machine as the status manager enables the status manager in Blelloch's device to consume messaging abilities. Fairfield taught a processor using three-state drivers (col.2, lines 4-16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blelloch, Chen and Papadopoulos and Fairfield because Fairfield's teaching of using three-state drivers help to employ feedback to the processor in Blelloch, Chen and Papadopoulos' system.

As to point (5), factual basis to the Official Notice taken were provided in Final Office Action dated on 10/15/2004.

In response to applicant's challenge in providing factual basis regarding claim 7 rejection, Blelloch taught to send acknowledgement to the status manager to inform task completion (col.3, lines 26-37). It is obvious to send notifications to notify the status manager of the current status. It would have been obvious to one of ordinary skill in the art at the time the invention was made to send a completion bit to the status manager in Blelloch and Papadopoulos' system to notify the completion of task execution in the system.

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In response to applicant's challenge in providing factual basis regarding claims 2-3 and 8 rejection, Van Dyke et al, US 6,412,070, filed September 21, 1998 disclose the use of KILL command (col.5, lines 25-35). This evidence proves that the Official Notice was properly taken and it would be obvious to provide KILL/Delete command in the system. It would have been obvious that the objective of a KILL/Delete action is to remove a specific instance. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a KILL action in Blelloch and Papadopoulos's system to clear a specific instance.

In response to applicant's challenge in providing factual basis regarding claims 5 and 9 rejection, Brown, US 3,914,744, filed January 2, 1973 disclosed a control register using L/R bit to direct the direction (col.3, lines 42-47). It would have been obvious to use CONFIG.L and CONFIG.R in Blelloch and Papadopoulos' system as the configuration registers to define the tasks, actions and instances.

Because Applicants have failed to challenge any of the Examiner's "Official Notices" stated in the previous office action in a proper and reasonably manner, they are now considered as admitted prior art. See MPEP 2144.03

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenny Lin whose telephone number is (571) 272-3968. The examiner can normally be reached on 8 AM to 5 PM Tue.-Fri. and every other Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ksl
July 26, 2005

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
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